Addressing the Operations Dilemma at Emerging Fabless Companies

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During initial SOC (System on Chip) design planning fundamental process, package, I.P. and design flow decisions are made. These decisions set the baseline for chip performance, system partitioning, cost, and identifying the primary suppliers. The focus at emerging companies is generally with system design, partitioning the system into the right ASIC components, chip design, EDA tools selection and project planning for the proof of concept. At this early stage the technology and supplier choices are made with the purpose of demonstrating working IC solutions. Unfortunately, what is often overlooked is that the ultimate company success is governed by the ability to manufacture the IC on time, at the right volumes and at the right cost points. It's true… new technologies enable new ideas… but unless attention is paid to making the right technology and partnership choices with production in mind the ultimate execution may fall short of expectations.

Virtual Operations

Recent publications[1,2] point to the need for a concurrent engineering approach and pro-active operations planning in order to avoid schedule delays. However, as discussed in a companion paper[3] most emerging companies face an "Operations" dilemma, in that staffing an operations function early is expensive, yet deferring it can cause ramp problems later. One solution is to leverage a Virtual Operations team in an outsourcing model.

Within the context of this paper "Operations" has a broader meaning than the activity and staffing solely to support the production ramp and execution. It also includes the tasks needed to support global planning, design support / operations planning, device prototyping and finally production execution. The tasks involved at each phase are outlined in Figure 1.

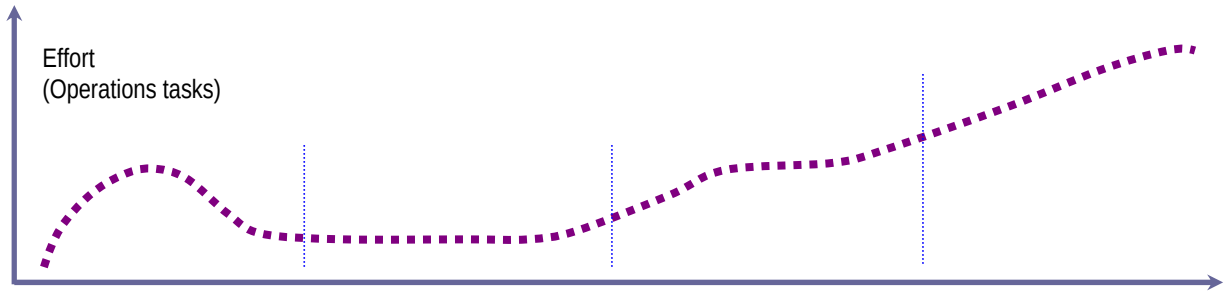
The required skills mix evolves between phases as depicted in Figure 2. The tasks during the global planning phase are primarily strategic and require technical, business and project planning skills. Establishing connections into the primary suppliers (foundry, assembly, I.P. / libraries etc.) is paramount. The Operations input into these decisions needs to be at a senior level, typically a "hands-on" V.P. function and / or a technology director level. Required elements of the team's strengths need to be:

- Technical skills in understanding the design requirements and matching them with the manufacturing technologies and supply chain.
- Business experience in helping make the right trade-offs, establishing and making connections with a solid supply chain including I.P. providers.
- Program Management skills to define a project plan that is aggressive yet achievable.

Figure 1. Operations Tasks During I.C. Productization

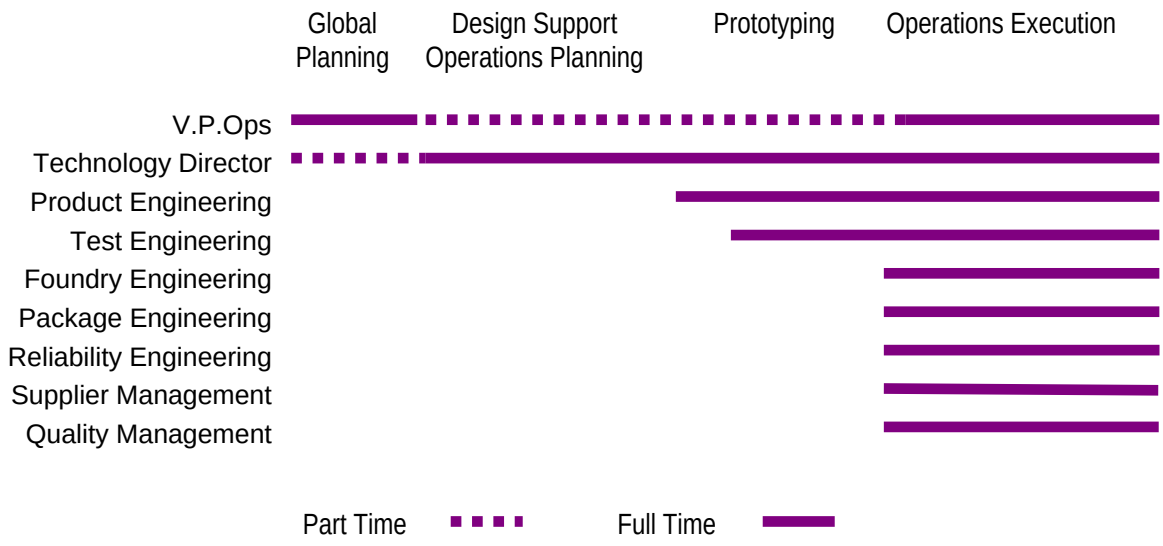
Productization Flow

System Design	Chip design	Prototyping	Qualification	Ramp



Global Planning	Design Support and Operations Planning	Prototyping & debug	Operations Execution
• Design methodology selection - ASSP, ASIC, COT or COT+ Design services • System partitioning optimization • Process and Package • Foundry and Assembly suppliers and early commits • Library, memory, I/O and embedded I.P. needs • Test platform and sources • Overall project planning through production • Generation of realistic cost estimates from data and trends • Provide realistic chip sizings and sensitivities	• Coordinate design deliverables, models, rules, packaging etc. • Negotiate library, I.P., supply chain contracts • Develop qualification / characterization plan • Review technology features and weigh cost trade-offs	• Coordination of tape out deliverables to fab • Coordination between fab, assembly for prototype delivery • Test H/W and test software development • Lifetest board design • ASIC debug, F/A • ASIC characterization	• Validation of yield and cost points • ASIC qualification • Transfer Final test to Production • Yield enhancement & cost reduction • Implement supplier management system • Implement Quality system and procedure based manufacturing

Figure 2. Operations Skills Needs Timeline



In the design support phase the primary tasks are to facilitate deliverables between foundry, assembly, I.P. suppliers and the internal design staff. Also in this period supplier contracts are negotiated and planning for prototyping logistics and device qualification are made. This function requires broad technical and business experience at the technical director level.

For the prototyping phase the Operations skills set requires the addition of product engineering to coordinate the tape-out deliverables, foundry and assembly logistics and troubleshooting and delivery of prototypes. The test engineering function is needed to coordinate test software and hardware for prototype delivery and ATE engineering. Coordinating design of necessary qualification hardware such as lifetest boards will be underway. Once prototypes are available system board level test, ASIC debug, ATE test and ASIC characterization will be coordinated by the Product Engineers.

In preparation for the production ramp the plan for implementing the full compliment of the Operations team will be underway. This is a transition to managing the revenue stream and includes managing the supply chain, managing the order entry and WIP control system, running the function under a quality system, improving the cost of goods and delivering to the sales forecast. This phase requires the full spectrum of Operations skills from the business level, supplier management and engineering sustaining functions.

A Sample – Things to look out for

A list of examples of potential gaps and traps that can become issues is provided in (Figure 3). The list is not exhaustive and is intended to highlight the value of an Operations perspective in the planning cycle. The list is most applicable to a “do-it yourself” COT model where the emerging company can take full advantage of the lower unit cost and flexibility of the COT model. In a traditional ASIC handoff some of the coordination issues become the responsibility of the ASIC supplier. The

Operations effort at the emerging company gets reduced but does not go away. It may also be important for the emerging company to use this list of concerns to ask the right questions and confirm that the issues are being addressed at the ASIC supplier – a good way to avoid "gaps".

Figure 3. A Sample of Areas of Concern – an Operations perspective

Process selection

Consider the maturity of the process – initially for the availability of stable models and eventually for manufacturing cost and delivery. For sure… 0.13um offers density and performance improvement relative to 0.18um… but beware of the escalating cost of masks. Although mask costs have come down figure on $500K-$700K for a production mask set at the 0.13um node. It is imperative that the design is right first time. Is a "shuttle" service available for device prototyping to save on NRE costs? Also… the 0.13um high-performance process trades device leakage for transistor drive strength and performance. At 0.13um and lower process nodes the transistor leakage can approach dynamic current levels. This is difficult to avoid and the associated problems do not diminish in static modes or with clock gating. This is a real challenge for devices targeted at low power or hand held applications.

In addition to cost and performance factors consider wafer pricing trends and market conditions. Weigh the defect density curve and incremental costs associated with design flexibility, i.e. added metal layers, MIMcaps, ESD implant etc. Consider the intercept point where leading or bleeding edge technologies will be stable for yield. Revolutionary process features typically take time to settle down and yield well.

Package selection

In addition to electrical, pinout and thermal performance consider also the costs and lead time associated with incremental items such as custom BGA substrate design. This is a frequent requirement for high performance designs where open tooling is most likely not available. Other considerations… are electrical models available for high frequency design? Are there sufficient power and ground resources to minimize IR drops and provide decoupling? What kind of package attach metallurgy is being used – will there be package to board assembly issues e.g. with tight BGA or TQFP lead pitch? As the die size estimates grow in the design phase will the package accommodate a larger die, a higher pin out or a higher thermal requirement?

Supplier selections

The reality is that engaging with the foundry and assembly suppliers is a two way street. Some foundries have formalized criteria for accepting business from new emerging clients. Is your fabless chip company positioned to be attractive to the choice suppliers? Has the supplier bought into the market, ramp plan, support requirements? One good test… Is the supplier willing to engage at the level of providing a customer number? i.e. to be recognized in their systems. Does the supplier adhere to accepted industry methods for qualifying the process and the package? Are there efficiencies in services? I.e. can the foundry do wafer probe if and when needed? Does the assembly house have the right test platform and capacity for final test? Will the assembly provider hold finished goods and mix / kit parts if necessary?

Library and I.P. provider selections

Has I.P. been verified in silicon? What are the licensing terms? What is the I.P. warranty?

Hard I.P. is generally tailored to specific processes. This will constrain foundry & process selection.

Consider testability factors. Does I.P. have BIST? Do the memory blocks have BIST, redundancy, repair capability for designs with large embedded memories?

Test platform

In addition to test platform capabilities for number of channels, speed, precision, analog instrumentation, test costs etc. consider also availability of the choice platform for test development and the source for production test. Is a test development source available locally? Where will production test be done? Is there adequate capacity on correctly configured testers?. There are often wide variations in tester configuration and availability within a given tester family. Where will final test be geographically located?

At what point does it make sense to implement wafer probe test?

Cost estimating

Include hidden yields and costs as follows:
Plan for a range of yields, yields predicted by fab models may not be achieved immediately. Consider that the chip may be pad limited and larger than expected. Die size estimates usually grow during design. Include wafer exclusion area, yield multiplier (Yo) term, defect improvement curve for yield modeling. Probe and final test costs should include derating for efficiency and indexing time. Include costs often overlooked – tray or tube cost, assembly yield, scan and bake cost, scan and bake yield, shipping costs, import / customs costs.

Decisions on use of available technology features

What is the optimal number of metal layers for your design? Does the I/O library assume the use of an optional ESD implant mask and corresponding cost increase?

Analog and RF circuits normally will require the use of optional masks or features such as MIMCAPS, reduced Vt transistors, resistors, optional thick metal for inductors etc. These need to be considered for costing and yield impact.

Qualification plan

Define the requirements… Specific use environments may have curtailed temperature, voltage or environmental operating ranges and therefore require characterization and qualification testing over a reduced range. This may save on qualification effort and costs. What are the customer requirements for average failure rate, early failure rate? Who will do the testing and what is the cost? Who will design and build lifetest boards? What other testing needs to be done? e.g. ESD testing.
How much can be leveraged from other sources such as the process qualification, package qualification, previous product qualifications etc.
Will there be a burn-in requirement or a need for elevated final testing to help screen for early failures?

Custom substrate / bonding diagrams

Performance driven or complex ASICs / SOC's may require the use of a custom designed substrate if they are to be assembled in a BGA to accommodate the power supply distribution scheme, optimal routing or signal trace matching. Consider the design costs, lead time, who will do the design and ownership of the custom inventory.

Coordinating tape-out deliverables to fab; Prototype logistics

Coordination of handoffs and documentation between foundry and assembly houses. Tape-out is a major milestone and cost commitment. Is there an adequate procedure or check list to make sure all the important design, test, quality, verification, debug factors have been addressed?
Is there a need to hold wafers for follow-up spins? At what point in the process?
What wafer splits are needed to represent process corners for the characterization effort?

ASIC debug, F/A (Failure Analysis)

What hooks are dialed into the physical design to help isolate problems? Such as landmarks or key nodes to top metal to help with FIB navigation and repair? With faster edges, lower supplies and large die sizes failures can be subtle and difficult to isolate.
Who will isolate whether an issue is process or design related? There is a tendency for the design team

to point at the process team and vice versa. Similarly with IP providers.
What recourse for corrective action exists with suppliers? Do they have resources to help with F/A? Is there a local resource equipped for decap of devices and to provide F/A services?

Conclusion

This paper outlines the Operations issues that must be considered proactively in order to set the foundation for smooth execution of IC development and manufacturing. Such issues are generally not a priority in initial design phases and can be a severe limiter as manufacturing is being scaled up. While there are many issues involved in the design and manufacturing of complex SOC ICs, a systematic approach to addressing these issues has been demonstrated by successful fabless IC companies. The challenge for emerging fabless companies is to manage the Operations Dilemma. A key to their success will be to leverage a broad-based and experienced team early in the development cycle.

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